CLAIMS

1. (previously amended) A semiconductor device comprising:

an interconnection board having first and second surfaces; and

a high rigidity plate securely fixed to and directly in contact with at least a majority of said second surface of said interconnection board,

said high rigidity plate being higher in rigidity than said interconnection board for suppressing said interconnection board from being bent upon receipt of any stress applied during at least a process for manufacturing said interconnection board.

2. (original) The semiconductor device as claimed in claim 1, wherein said interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure.

3. (original) The semiconductor device as claimed in claim 1, wherein said high rigidity plate is made of a metal.

4. (original) The semiconductor device as claimed in claim 1, wherein said high rigidity plate is made of an alloy.

5. (original) The semiconductor device as claimed in claim 1, wherein said high rigidity plate is made of a ceramic.

6. (original) The semiconductor device as claimed in claim 1, wherein a base material of said interconnection board is an organic insulative material.

7. (original) The semiconductor device as claimed in claim 6, wherein said organic material is a polymer resin material.

8. (previously amended) A semiconductor device comprising:

an interconnection board having first and second surfaces;

at least one semiconductor chip mounted on said first surface of said interconnection board; and

a high rigidity plate securely fixed to and directly in contact with at least a majority of said second surface of said interconnection board,

said high rigidity plate being higher in rigidity than said interconnection board for suppressing said interconnection board from being bent upon receipt of any stress applied during at least processes for manufacturing said interconnection board

and for mounting said at least one semiconductor chip on said first surface.

9. (original) The semiconductor device as claimed in claim 8, wherein said interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure.

10. (original) The semiconductor device as claimed in claim 8, wherein said high rigidity plate is made of a metal.

11. (original) The semiconductor device as claimed in claim 8, wherein said high rigidity plate is made of an alloy.

12. (original) The semiconductor device as claimed in claim 8, wherein said high rigidity plate is made of a ceramic.

13. (original) The semiconductor device as claimed in claim 8, wherein a base material of said interconnection board is an organic material.

14. (original) The semiconductor device as claimed in claim 13, wherein said organic material is a polymer resin material.

15. (original) The semiconductor device as claimed in claim 8, wherein said at least semiconductor chip is bonded via bumps to said second surface of said interconnection board.

16. (original) The semiconductor device as claimed in claim 15, wherein further comprising a sealing resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

17. (original) The semiconductor device as claimed in claim 16, further comprising at least a heat spreader provided on said at least semiconductor chip.

18. (currently amended) A semiconductor device comprising:

an interconnection board having first and second surfaces;

at least one external electrode pad buried in said interconnection board,

said at least one external electrode pad having an exposed surface level with said second surface so that said second surface and said exposed surface form a single flat plane;

at least a semiconductor chip mounted on said first surface of said interconnection board; and

[a] buffer layer means having a first surface in contact with said second surface of said interconnection board and [also said buffer layer having] a second surface on which at least one external electrode is provided, [and] said buffer layer means for providing at least one electrical contact between said one external electrode pad and said at least one external electrode[,] and for [said buffer layer being capable of] absorbing and/or relaxing a stress applied to said at least external electrode to make said interconnection board free from application of said stress.

19. (original) The semiconductor device as claimed in claim 18, wherein said interconnection board comprises a multilayer interconnection board having a multilevel interconnection structure.

20. (original) The semiconductor device as claimed in claim 18, wherein said at least external electrode comprises plural external electrodes.

21. (original) The semiconductor device as claimed in claim 18, wherein said external electrode comprises a solder ball.

22. (original) The semiconductor device as claimed in claim 18, wherein said external electrode comprises a pin electrode.

23. (original) The semiconductor device as claimed in claim 18, wherein said external electrode comprises a coil-spring electrode.

24. (original) The semiconductor device as claimed in claim 18, wherein said external electrode comprises a generally column shaped electrode.

25. (original) The semiconductor device as claimed in claim 24, wherein said generally column shaped electrode comprises a straight column shaped electrode which is uniform in horizontal cross sectional area from a bottom to a top thereof.

26. (original) The semiconductor device as claimed in claim 24, wherein said generally column shaped electrode comprises a center-pinched column shaped electrode which decreases in horizontal cross sectional area toward an intermediate level thereof.

27. (currently amended) The semiconductor device as claimed in claim 18, wherein said buffer layer <u>means</u> comprises:

plural generally column shaped electrically conductive layers, each of which has a first end fixed to an external electrode pad of said interconnection board and a second end directly fixed said external electrode.

28. (original) The semiconductor device as claimed in claim 27, wherein said plural generally column shaped electrically conductive layers are made of a metal.

29. (currently amended) The semiconductor device as claimed in claim 18, wherein said buffer layer means comprises:

plural generally column shaped electrically conductive layers, each of which has a first end fixed to an external electrode pad of said interconnection board and a second end directly fixed said external electrode; and

an stress absorption layer filling gaps between said plural generally column shaped electrically conductive layers, and said stress absorption layer being lower in rigidity than said plural generally column shaped electrically conductive layers, and said stress absorption layer surrounding said plural generally column shaped electrically conductive layers so that said stress absorption layer is in tightly contact with said plural generally column shaped electrically conductive layers.

30. (original) The semiconductor device as claimed in claim 29, wherein said plural generally column shaped electrically conductive layers are made of a metal.

31. (original) The semiconductor device as claimed in claim 29, wherein said stress absorption layer is made of an organic insulative material.

32. (currently amended) The semiconductor as claimed in claim 18, wherein said buffer layer means comprises:

plural generally column shaped electrically conductive layers, each of which has a first end fixed to an external electrode pad of said interconnection board and a second end directly fixed said external electrode;

a supporting plate having plural holes, into which said plural generally column shaped electrically conductive layers with said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said interconnection board to form an inter-space between said supporting plate and said second surface of said interconnection board; and

a supporting sealing resin material filling said inter-space and surrounding both said plural generally column shaped electrically conductive layers and parts of said external electrodes so that said supporting sealing resin material is in

tightly contact with said plural generally column shaped electrically conductive layers and said parts of said external electrodes for supporting said external electrodes.

33. (original) The semiconductor device as claimed in claim 32, wherein said supporting sealing resin material is lower in rigidity than said plural generally column shaped electrically conductive layers so that said supporting sealing resin material is capable of absorbing and/or relaxing a stress applied to said external electrodes.

34. (original) The semiconductor device as claimed in claim 32, wherein said plural generally column shaped electrically conductive layers are made of a metal.

35. (original) The semiconductor device as claimed in claim 32, wherein said supporting sealing resin material is made of an organic insulative material.

36. (currently amended) The semiconductor device as claimed in claim 18, further comprising a supporting layer on said second surface of said buffer layer means for supporting said external electrode.

37. (currently amended) The semiconductor device as claimed in claim 36, wherein said supporting layer further comprises:

a supporting plate having plural holes into which holes said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said buffer layer means to form an inter-space between said supporting plate and said second surface of said buffer layer means; and

a supporting sealing resin material filling said inter-space and surrounding parts of said external electrodes so that said supporting sealing resin material is in tight contact with said parts of said external electrodes for supporting said external electrodes.

38. (previously amended) The semiconductor device as claimed in claim 18, wherein said at least semiconductor chip is bonded via bumps to said first surface of said interconnection board.

39. (original) The semiconductor device as claimed in claim 38, wherein further comprising a sealing resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

40. (original) The semiconductor device as claimed in claim 39, further comprising at least a heat spreader provided on said at least semiconductor chip.

41. (original) The semiconductor device as claimed in claim 38, wherein further comprising an under-fill resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

42. (currently amended) The semiconductor device as claimed in claim 41, further comprising:

a stiffener extending on a peripheral region of said buffer layer means; and

at least a heat spreader provided on said at least semiconductor chip and on said stiffener.

43. (currently amended) A semiconductor device comprising:

an interconnection board having first and second surfaces;

at least one external electrode pad buried in said interconnection board,

said at least one external electrode pad having an exposed surface level with said second surface so that said second surface and said exposed surface form a single flat plane;

at least a semiconductor chip mounted on said first surface of said interconnection board;

at least one external electrode fixed to said at least one external electrode pad; [and]

a supporting layer on said second surface of said interconnection board for supporting said external electrodes

a buffer layer having a first surface in contact with said second surface of said interconnection board, and

wherein said supporting layer further comprises

a supporting plate having plural holes into which holes said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said buffer layer to form an inter-space between said supporting plate and said second surface of said buffer layer; and

a supporting sealing resin material filling said inter-space and surrounding parts of said external electrodes so that said supporting sealing resin material is in tight contact with said parts of said external electrodes.

44. (canceled)

45. (previously amended) The semiconductor device as claimed in claim 43, wherein said at least semiconductor chip is

bonded via bumps to said first surface of said interconnection board.

46. (original) The semiconductor device as claimed in claim 45, wherein further comprising a sealing resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

47. (original) The semiconductor device as claimed in claim 46, further comprising at least a heat spreader provided on said at least semiconductor chip.

48. (original) The semiconductor device as claimed in claim 45, wherein further comprising an under-fill resin material provided on said first surface of said interconnection board for sealing said at least semiconductor chip and said bumps.

49. (currently amended) The semiconductor device as claimed in claim 48, further comprising:

[a buffer layer having a first surface in contact with said second surface of said interconnection board;]

a stiffener extending on a peripheral region of said buffer layer; and

at least a heat spreader provided on said at least semiconductor chip and on said stiffener.

50. (original) The semiconductor device as claimed in claim 43, wherein said external electrodes connected through plural generally column shaped electrically conductive layers to external electrode pads on said second surface of said interconnection board, and said supporting layer further comprises:

a supporting plate having plural holes, into which said plural generally column shaped electrically conductive layers with said external electrodes are inserted, and said supporting plate extending in parallel to said second surface of said interconnection board to form an inter-space between said supporting plate and said second surface of said interconnection board; and

a supporting sealing resin material filling said inter-space and surrounding both said plural generally column shaped electrically conductive layers and parts of said external electrodes so that said supporting sealing resin material is in tightly contact with said plural generally column shaped electrically conductive layers and said parts of said external electrodes for supporting said external electrodes.

51. (original) The semiconductor device as claimed in claim 50, wherein said supporting sealing resin material is lower in rigidity than said plural generally column shaped electrically conductive layers so that said supporting sealing resin material

is capable of absorbing and/or relaxing a stress applied to said external electrodes.

52. (original) The semiconductor device as claimed in claim 50, wherein said plural generally column shaped electrically conductive layers are made of a metal.

53. (original) The semiconductor device as claimed in claim 50, wherein said supporting sealing resin material is made of an organic insulative material.

54. (original) The semiconductor device as claimed in claim 43, wherein said external electrode comprises a solder ball.

55. (original) The semiconductor device as claimed in claim 43, wherein said external electrode comprises a pin electrode.

56. (original) The semiconductor device as claimed in claim 43, wherein said external electrode comprises a coil-spring electrode.

57. (original) The semiconductor device as claimed in claim 18, wherein said external electrode comprises a generally column shaped electrode.

58. (original) The semiconductor device as claimed in claim 24, wherein said generally column shaped electrode comprises a straight column shaped electrode which is uniform in horizontal cross sectional area from a bottom to a top thereof.

59. (original) The semiconductor device as claimed in claim 24, wherein said generally column shaped electrode comprises a center-pinched column shaped electrode which decreases in horizontal cross sectional area toward an intermediate level thereof.

60. - 79. (canceled)

80. (previously added) A semiconductor device comprising:

an interconnection board having first and second surfaces;

at least one external electrode pad buried in said interconnection board,

said at least one external electrode pad having an exposed surface level with said second surface so that said

second surface and said exposed surface form a single flat plane; and

a high rigidity plate securely fixed to and directly contact with at least a majority of said single flat plane,

said high rigidity plate being higher in rigidity than said interconnection board and suppressing said interconnection board from being bent.

81. (previously added) The semiconductor device as claimed in claim 80, wherein said high rigidity plate is securely fixed to and directly in contact with an entirety of said single flat plane.

82. (previously added) A semiconductor device comprising:

an interconnection board having first and second surfaces;

at least one external electrode pad buried in said interconnection board,

said at least one external electrode pad having an exposed surface level with said second surface so that said second surface and said exposed surface form a single flat plane;

at least a semiconductor chip mounted on said first surface of said interconnection board; and

a high rigidity plate securely fixed to and directly contact with at least a majority of said single flat plane,

said high rigidity plate being higher in rigidity than said interconnection board and suppressing said interconnection board from being bent.

83. (previously added) The semiconductor device as claimed in claim 82, wherein said high rigidity plate is securely fixed to and directly contact with an entirety of said single flat plane.

84. (previously added) The semiconductor device as claimed in claim 1, wherein said high rigidity plate is securely fixed to and directly contact with an entirety of said second surface.

85. (previously added) The semiconductor device as claimed in claim 8, wherein said high rigidity plate is securely fixed to and directly contact with an entirety of said second surface.